REMARKS

Summary of Claim Status

Claims 1-10 are pending in the present application after entry of the present amendment. Claims 1–10 are rejected for the reasons discussed below. Applicant respectfully requests favorable reconsideration of the claims and withdrawal of the pending rejections in view of the present amendment and in light of the following discussion.

Rejections Under 35 U.S.C. § 102

Claims 1-2 and 5-9 are rejected under 35 U.S.C. § 102(b) as being anticipated by Hayashi et al., U.S. Patent No. 4,980,308 ("Hayashi"). Claims 1 and 4 are rejected under 35 U.S.C. § 102(e) as being anticipated by Ishikawa, U.S. Patent No. 6,682,963 ("Ishikawa"). Applicant respectfully traverses these rejections.

Applicant has voluntarily amended Claim 1, believed to be allowable without amendment, merely to make explicit what was inherent in the claim as originally filed. In particular, Applicant has amended Claim 1 to recite "wherein the island extends outward from a back side surface of the interconnect portion opposite the face side surface of the device wafer portion." Neither Hayashi nor Ishikawa disclose or teach the features of Claim 1.

The Examiner alleges that Fig. 2 of Hayashi teaches a source region (35sa), a drain region (35da) and a channel structure. However, the Office Action does not assert, much less prove, that Hayashi teaches or even suggests that the source region, the drain region, and the channel structure together form an island of a semiconductor material as recited in Claim 1. Nowhere does Hayashi even mention, much less teach, an island of semiconductor material, or any similar concept.

Fig. 2 of Hayashi merely shows a semiconductor device where a portion of the substrate is etched or ground flat to allow for wiring layers on both surfaces of the semiconductor. As noted in Hayashi, it is important for the surface where wiring layer 6 is deposited to be made flat "to avoid that the wiring stage is broken off by the

uneveness." Hayashi at col. 5, lines 35-42. That is, Hayashi requires that the surface of the semiconductor be etched or ground flat so that reliability problems in the wiring layer due to breaks can be avoided, and therefore teaches away from a surface that is not flat. Thus, Hayashi describes a device having source, drain, and channel regions that are etched flat with the surrounding material, e.g., insulating layer 52.

Similarly, the Office Action fails to assert or prove that Ishikawa teaches, or even suggests, that the source, drain, and channel together form an island of a semiconductor material as recited in Claim 1. Figs. 9 and 10 of Ishikawa merely describe a thin film transistor for use in an active matrix display where a portion of the device is removed to form a flat surface (e.g., Figs. 10A and 10B). As stated above, Ishikawa does not even mention, much less teach or disclose islands of semiconductor material. In Ishikawa, the surfaces of the wafer are flat, so there is certainly no teaching that the islands extend outward from a back side surface of an interconnect portion.

In contrast, Claim 1 recites that the island extends outward from the back side surface, thereby resulting in a surface that is not flat. For example, Fig. 16 of the present application shows an example of an island that extends outward from the back side surface of the interconnect portion. Neither Hayashi nor Ishikawa teach or even suggest such an island. Therefore, Applicant respectfully submits that Claim 1, as amended, is allowable, and allowance of Claim 1 is respectfully requested.

Claims 2 and 4-7 depend from Claim 1 and thus include all of the limitations of Claim 1. Applicant believes Claim 1 is allowable for the reasons set forth above. Therefore, for at least the same reasons, Applicant believes Claims 2 and 4-7 are also allowable, and allowance of such claims is respectfully requested.

With respect to Claim 8, the Examiner states that the source region corresponds to element 35sa of Hayashi and the means corresponds to the channel of Hayashi. Applicant has voluntarily amended Claim 8 to recite: "the device wafer having a back side opposite the face side, wherein at least one surface of at least one of the source region and the drain region substantially normal to the back side is

exposed." Applicant respectfully submits that Hayashi does not teach or disclose at least this feature.

Fig. 2B of Hayashi shows a semiconductor device having source and drain regions that are entirely surrounded and not exposed externally at all. For instance, source region 35sa of Hayashi is completely surrounded by insulating layers 4 and 52, an n- channel, and a wiring layer 6. Source and drain regions 35da, 35sb, and 35db of Hayashi are similarly surrounded, and therefore not exposed. Furthermore, all surfaces of the source and drain regions of Hayashi normal to the back side are formed adjacent to insulating layer 52. Thus, these normal surfaces are not taught or disclosed by Hayashi to be exposed, but are instead covered by an insulating layer. As noted in Hayashi, the insulating layer 52 is needed to separate the p-MIS and the n-MIS. Hayashi at col. 5, lines 7-8.

In contrast, Applicant recites in Claim 8 that at least one surface of at least one of the source region and the drain region normal to a back side of the wafer is exposed. For example, as shown in Fig. 15 and described in the corresponding text, an etching step may be performed to remove material outside a mask boundary. As shown in the example of Fig. 16, this etching may remove a portion of a well or substrate region, thereby leaving behind an exposed surface normal to the back side. Hayashi does not teach, or even suggest, such a surface. Therefore, Applicant respectfully submits that Claim 8 is allowable over Hayashi, and respectfully requests allowance of Claim 8.

Claim 9 depends from Claim 8 and thus includes all of the limitations of Claim 8. Applicant believes Claim 8 is allowable for the reasons set forth above. Therefore, for at least the same reasons, Applicant believes Claim 9 is also allowable, and allowance of Claim 9 is respectfully requested.

All of the above amendments are fully supported by the specification, for example in Figs. 15 and 16 and the corresponding text.

Rejections Under 35 U.S.C. § 103

Claims 3 and 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hayashi in view of Matsumoto et al., U.S. Patent No. 6,794,717 ("Matsumoto"). Claim 3 depends from Claim 1, and Claim 10 depends from Claim 8. For the reasons set forth above, Applicant believes Claims 1 and 8 are allowable. Furthermore, Matsumoto does not overcome the deficiencies of Hayashi. Therefore, for at least the same reasons, Applicant believes Claims 3 and 10, respectively, are also allowable, and allowance of Claims 3 and 10 is respectfully requested.

Conclusion

No new matter has been introduced by any of the above amendments. In light of the above amendments and remarks, Applicant believes that Claims 1-10 are in condition for allowance, and allowance of the application is therefore respectfully requested. If action other than allowance is contemplated by the Examiner, the Examiner is invited to telephone Applicant's attorney, Justin Liu, at 408-879-4641.

Respectfully submitted,

Justin Liu
Attorney for Applicant
Reg. No. 51,959

I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450, on April 29, 2005.

Julie Matthews
Name

Signature